AMENDMENTS TO THE CLAIMS

1. (Currently amended) A MOS transistor comprising:

an isolation layer formed at a predetermined region of a semiconductor substrate to define an active region;

an upper trench region formed in the active region, the upper trench region crossing the active region to divide the active region into two sub-active regions;

a spacer covering at least a pair of sidewalls of the upper trench region that are adjacent to the active region;

a lower trench region formed under the upper trench region surrounded by the spacer;

a pair of a low concentration source/drain region formed under the spacer, the low concentration source/drain regions being shallower than the lower trench region;

a pair of high concentration source/drain regions formed at top surfaces of the sub-active regions that are located at both sides of the upper trench region respectively;

a gate insulating layer covering the sidewalls and a bottom surface of the lower trench region; and

a gate electrode filling the lower trench region, surrounded by the gate insulating layer, and filling the upper trench region, surrounded by the spacer.

2. (Original) The MOS transistor of claim 1, wherein the upper trench region has a greater width than the active region.

3. (Original) The MOS transistor of claim 1, wherein the spacer comprises a first spacer adjacent to the active region and a second spacer adjacent to the isolation layer, the first spacer having the same width as the second spacer.

4. (Original) The MOS transistor of claim 3, wherein the upper trench region has a width that is equal to or greater than the sum of twice width of the second spacer and the width of the active region

5. (Currently amended) The MOS transistor of claim 3 ~~further comprising a pair of low concentration source/drain regions formed~~ wherein the pair of low concentration source regions are formed in the semiconductor substrate under the first spacer, and formed in contact with sidewalls of the lower trench region.

6. (Original) The MOS transistor of claim 1, wherein the lower trench region has the same width as the active region.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (New) The MOS transistor of claim 3, wherein the second spacer is located orthogonal to the first spacer.